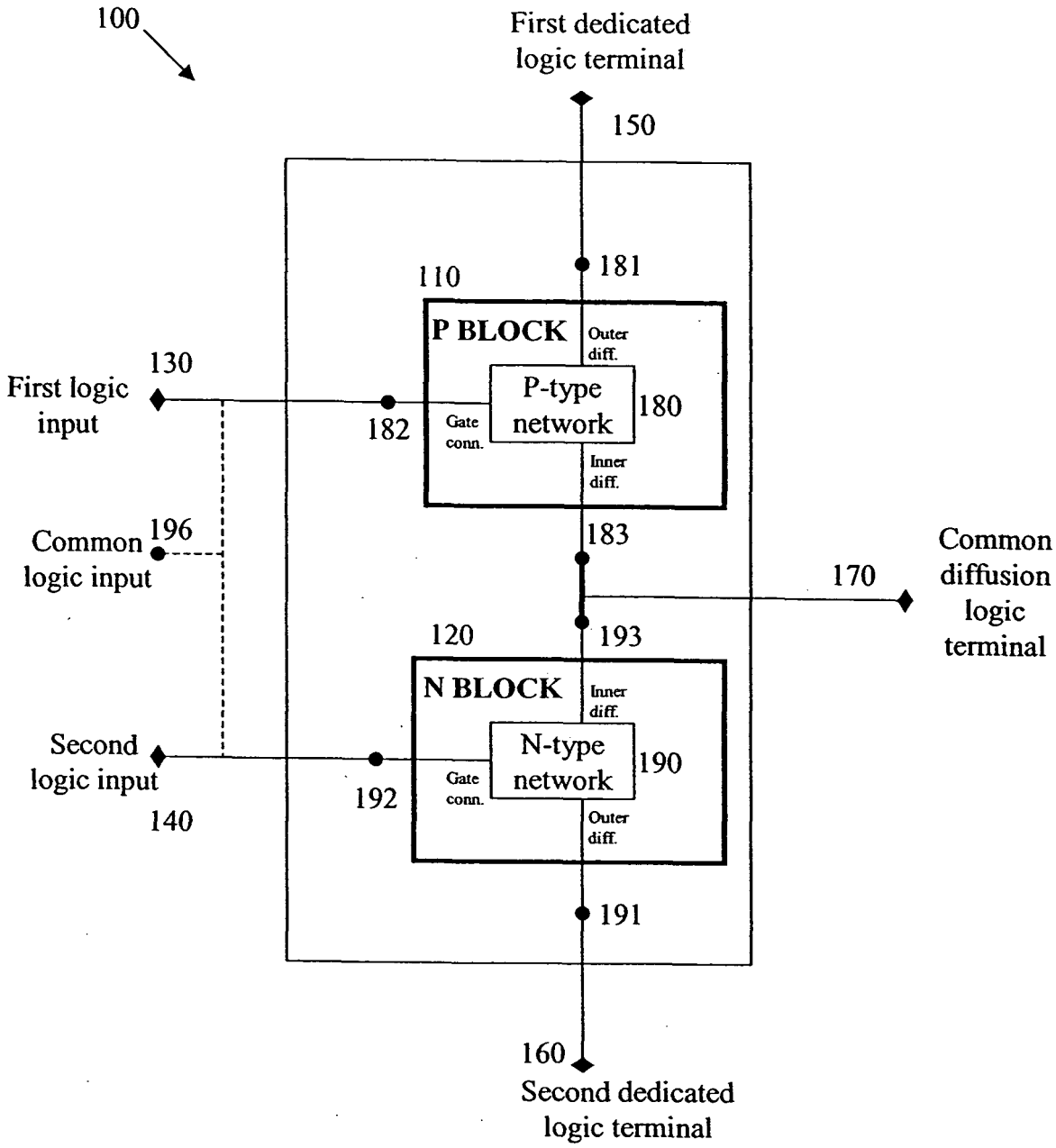

100
First dedicated logic terminal
150
181
110
P BLOCK
Outer diff.
130
First logic input
P-type network
180
182
Gate conn.
Inner diff.
Common 196
logic input
183
170
Common diffusion logic terminal
120
193
N BLOCK
Inner diff.
Second logic input
N-type network
190
192
Gate conn.
140
Outer diff.
191
160
Second dedicated logic terminal

Figure 1

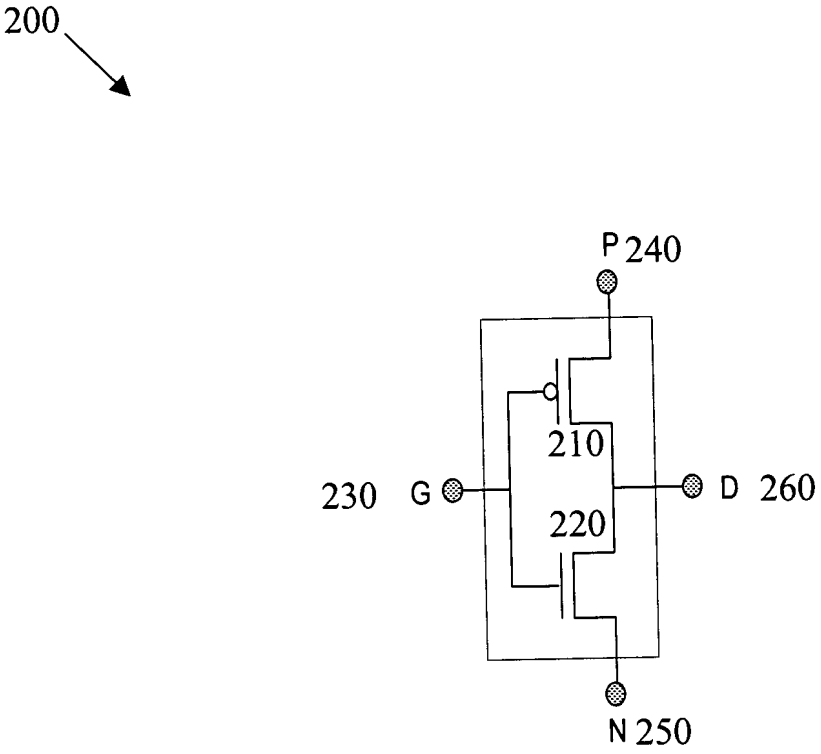


Figure 2

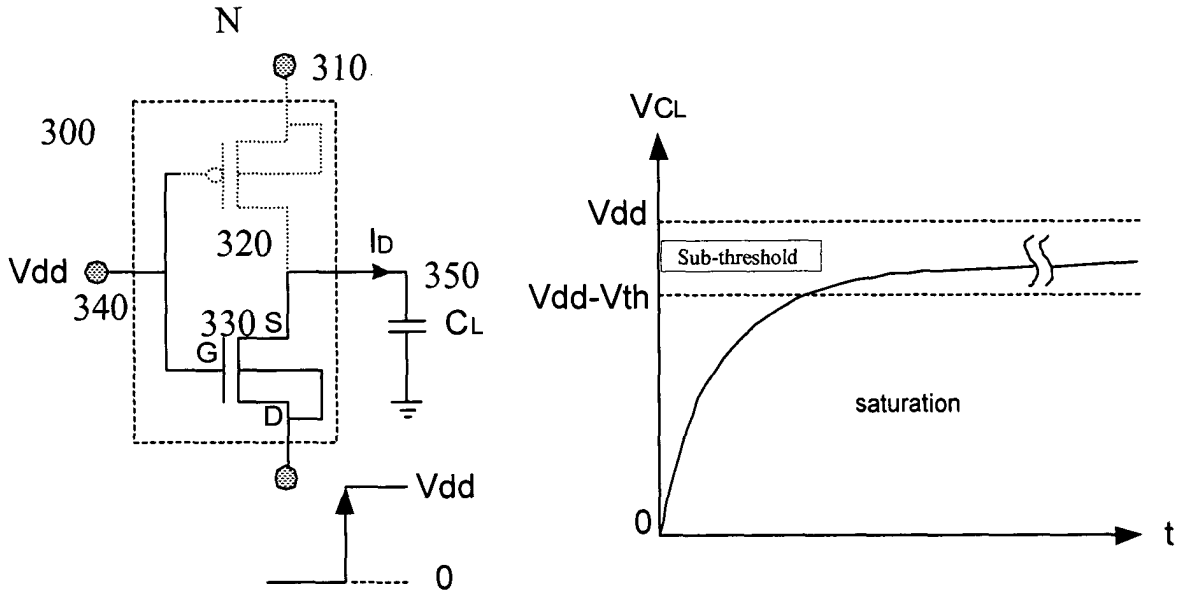

N
310
300
320
ID
Vdd
340
350
330 S
G
CL
D
Vdd
0
VCL
Vdd
Sub-threshold
Vdd-Vth
saturation
0
t

Figure 3

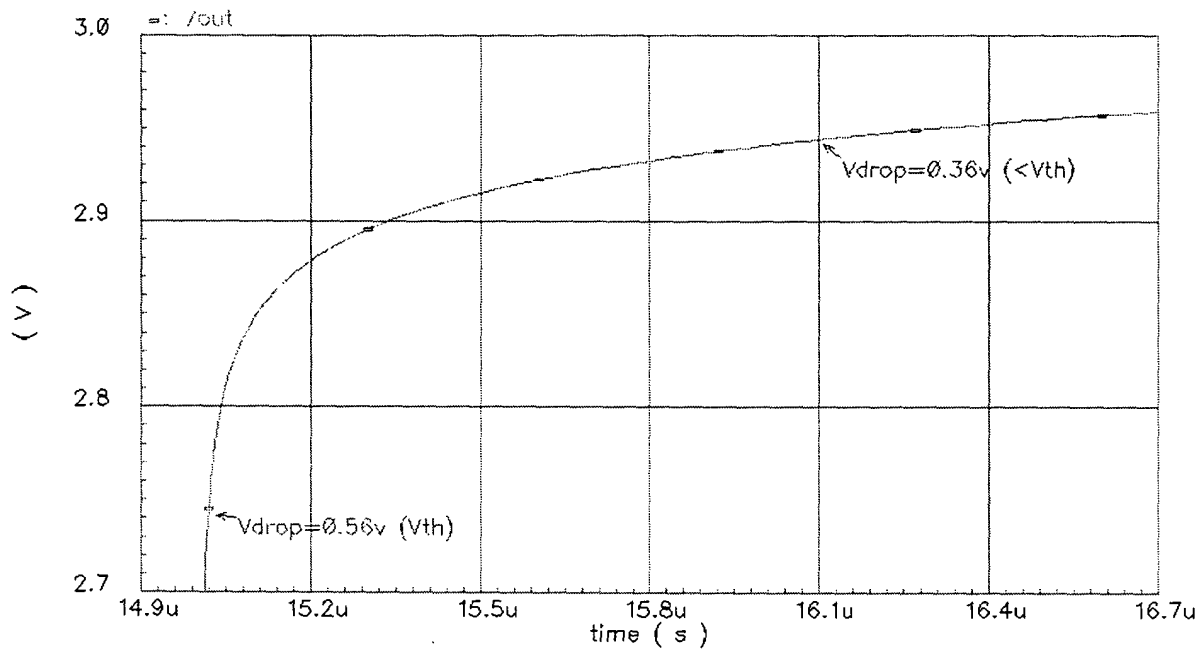

3.0
=: /out
2.9
2.8
2.7
(V)
Vdrop=0.36v (<Vth)
Vdrop=0.56v (Vth)
14.9u
15.2u
15.5u
15.8u
16.1u
16.4u
16.7u
time (s)

Figure 4

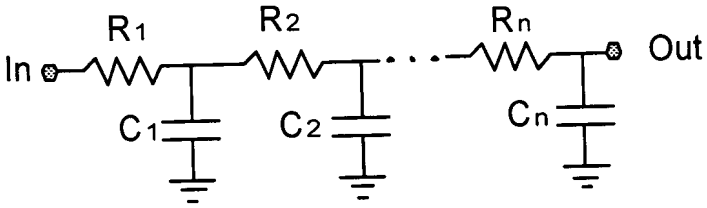


Figure 5

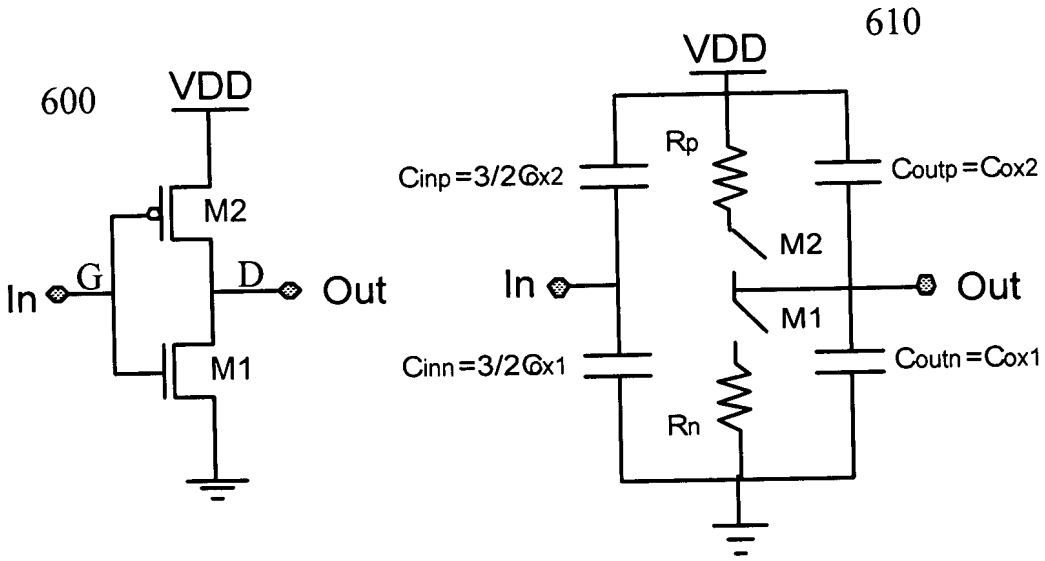

600
VDD
M2
In
G
D
Out
M1
610
VDD
Rp
Cinp=3/2Cox2
Coutp=Cox2
M2
In
Out
M1
Cinn=3/2Cox1
Coutn=Cox1
Rn

Figure 6

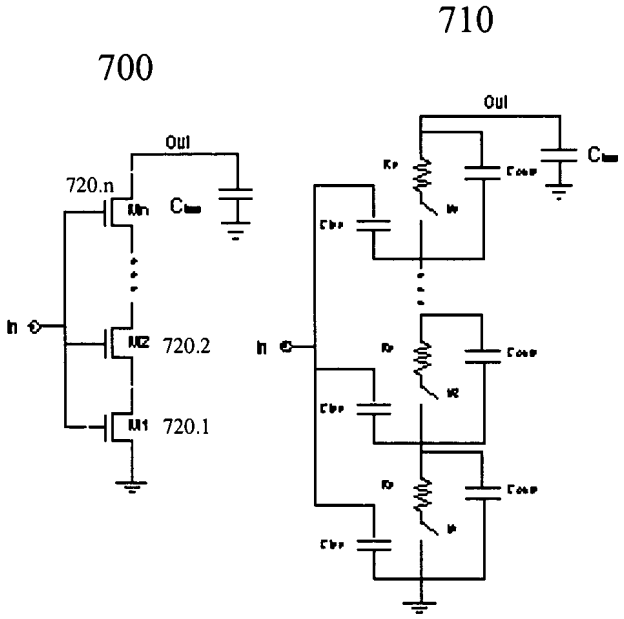


Figure 7 - Prior art

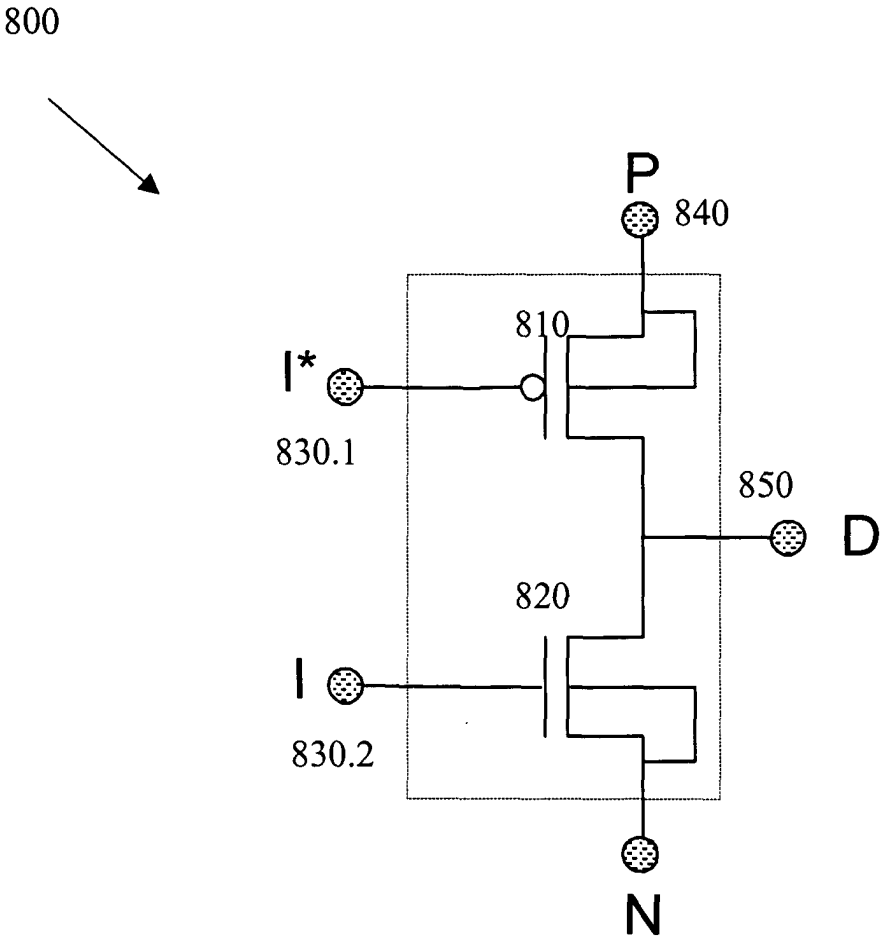


Figure 8

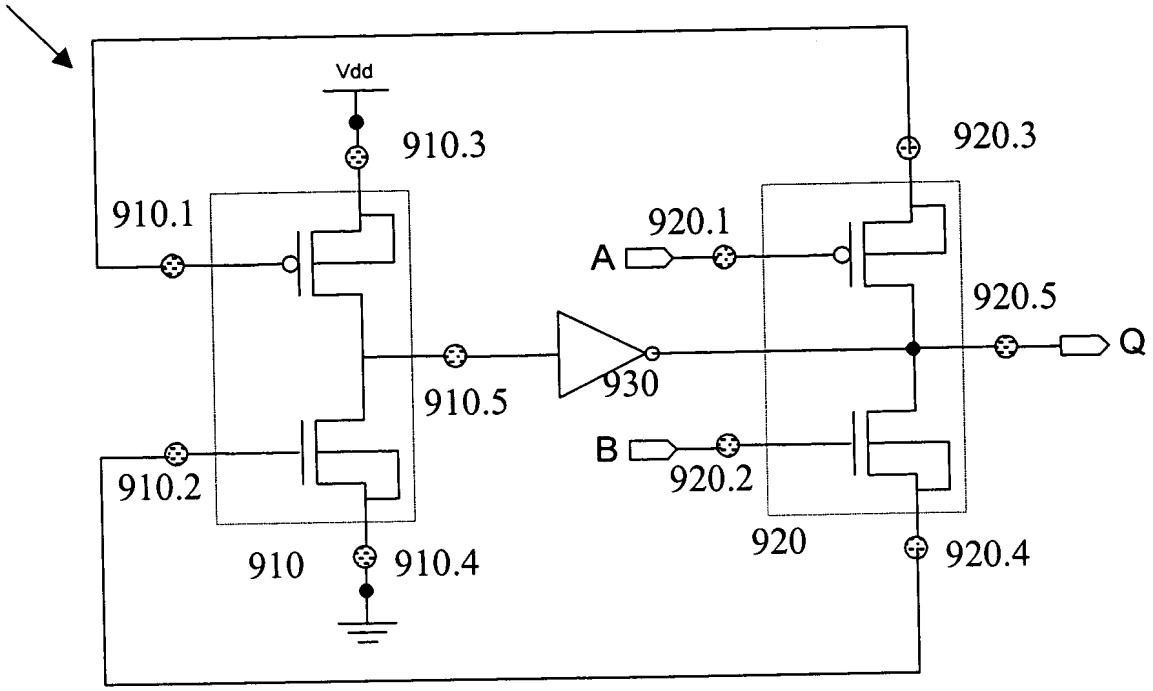

900
Vdd
910.3
910.1
910.5
910.2
910
910.4
930
920.3
920.1
A
920.5
Q
B
920.2
920
920.4

Figure 9

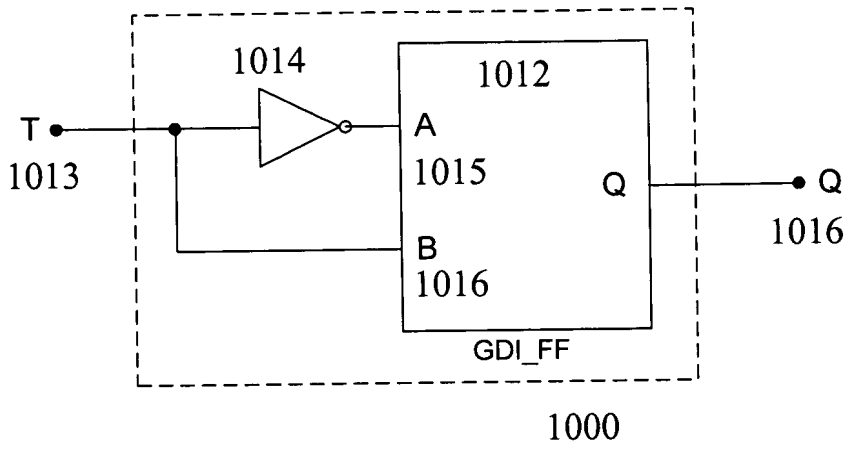


Figure 10a

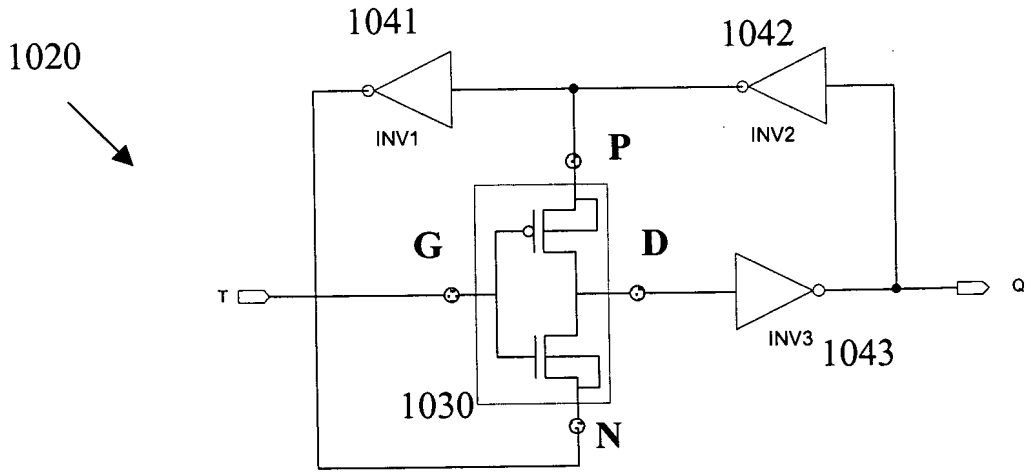


Figure 10b

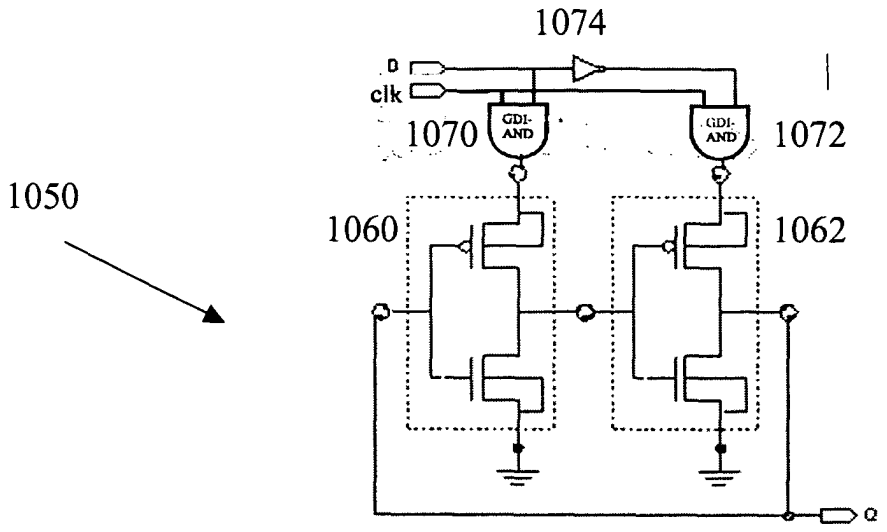


Figure 10c

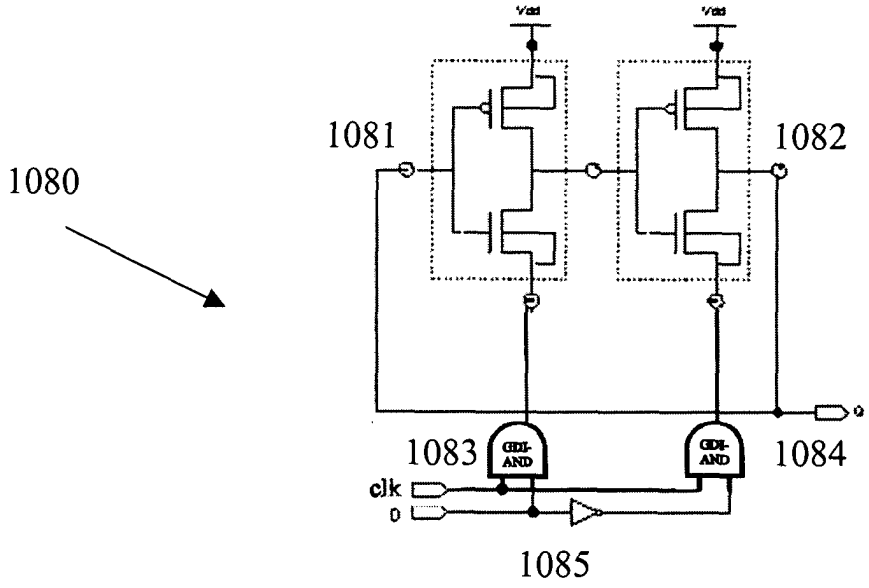


Figure 10d

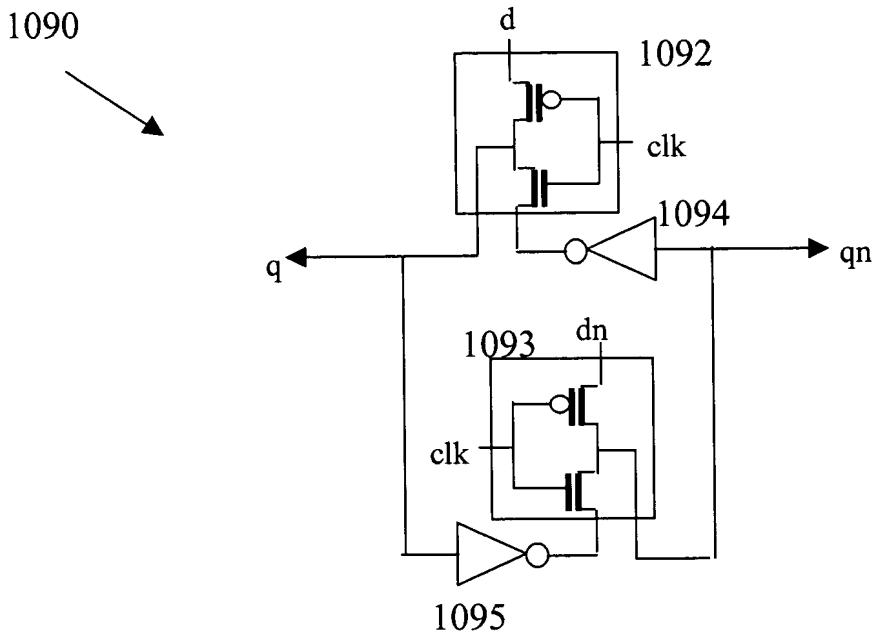


Figure 10e

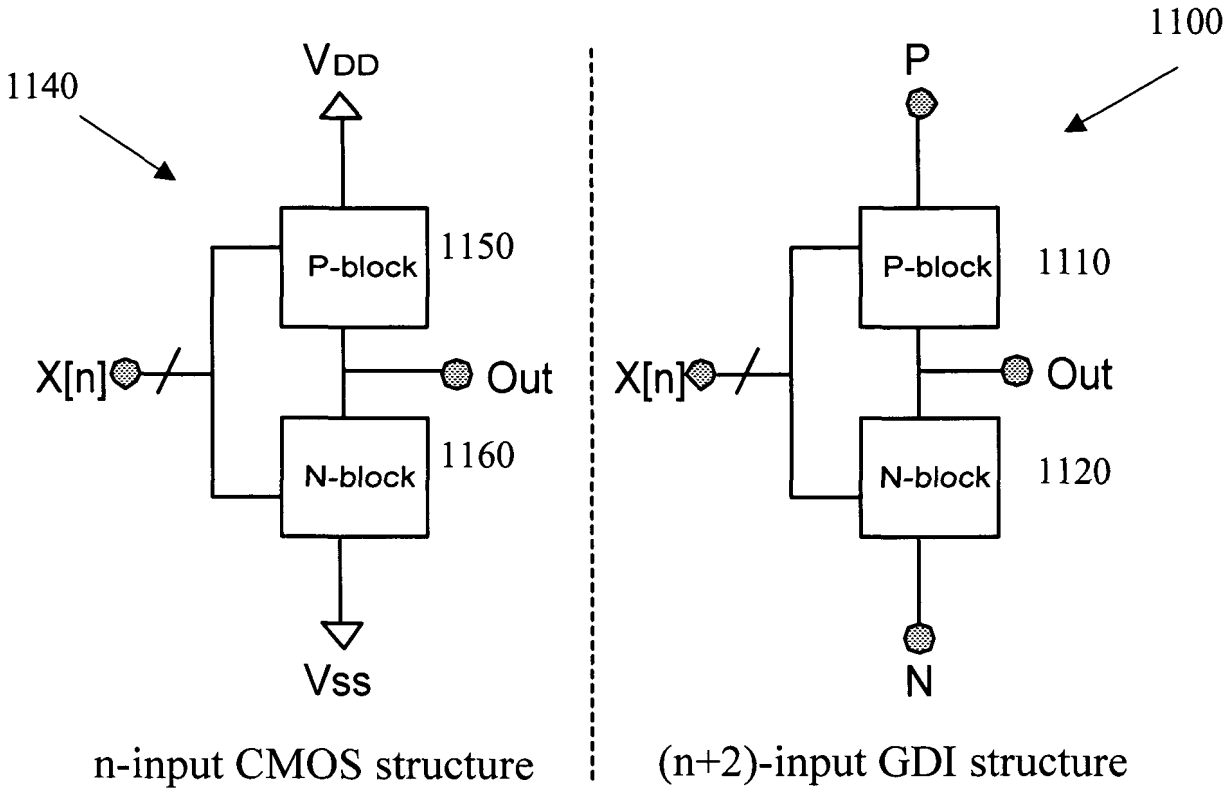
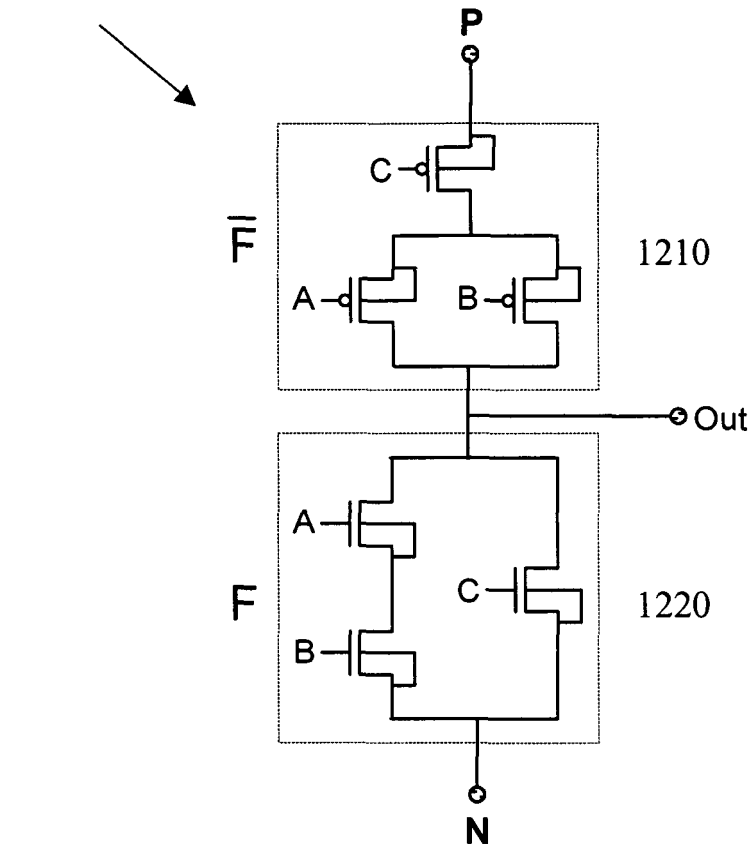

1140
VDD
P-block
1150
X[n]
Out
N-block
1160
Vss
n-input CMOS structure
1100
P
P-block
1110
X[n]
Out
N-block
1120
N
(n+2)-input GDI structure

Figure 11



$Out=\overline{F}P+FN=\overline{(AB+C)}P+(AB+C)N$

Figure 12

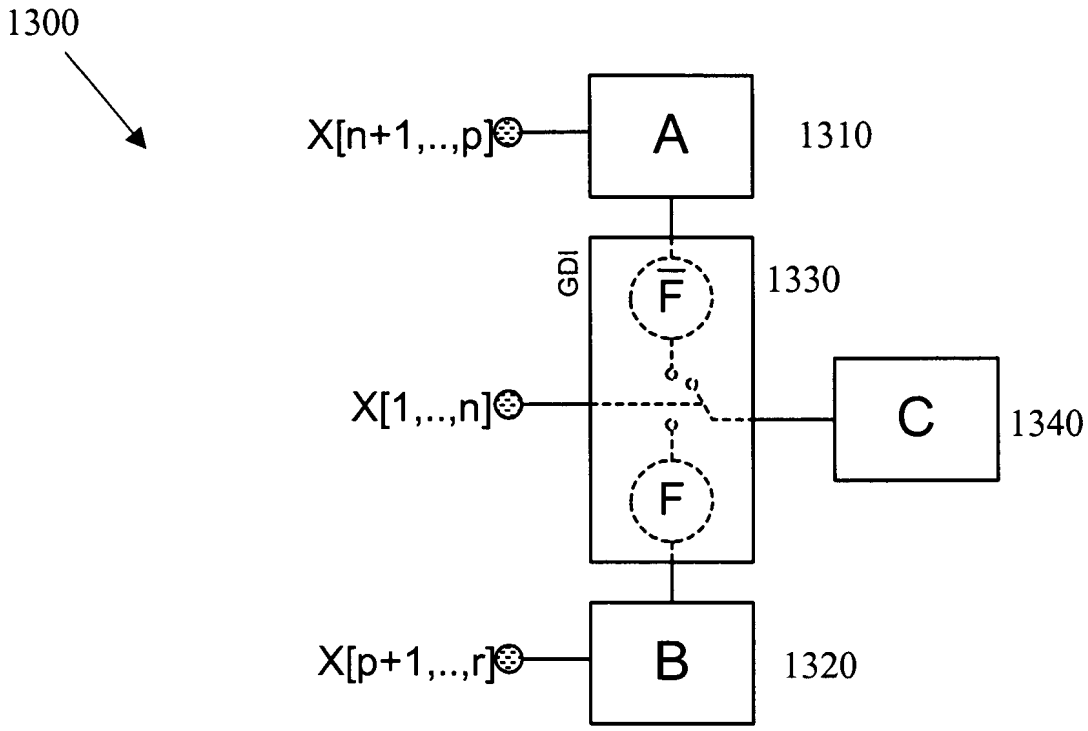


Figure 13

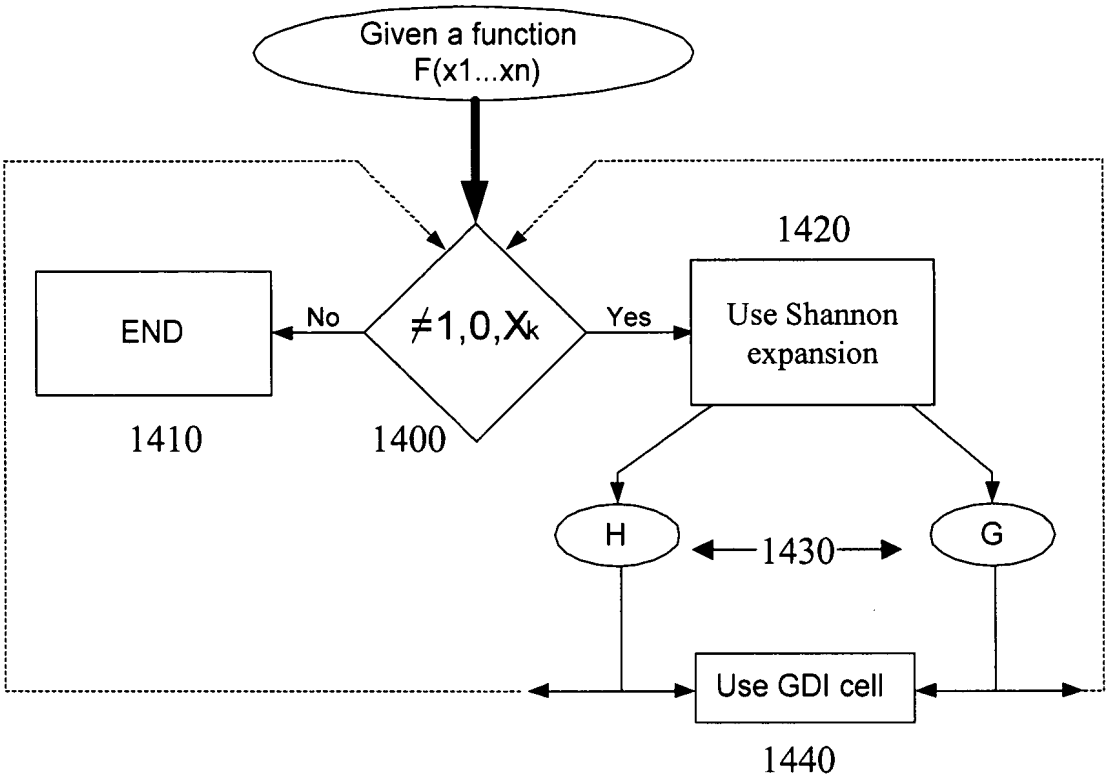

Given a function
F(x1...xn)
1420
END
No
≠1,0,Xk
Yes
Use Shannon
expansion
1410
1400
H
1430
G
Use GDI cell
1440

Figure 14

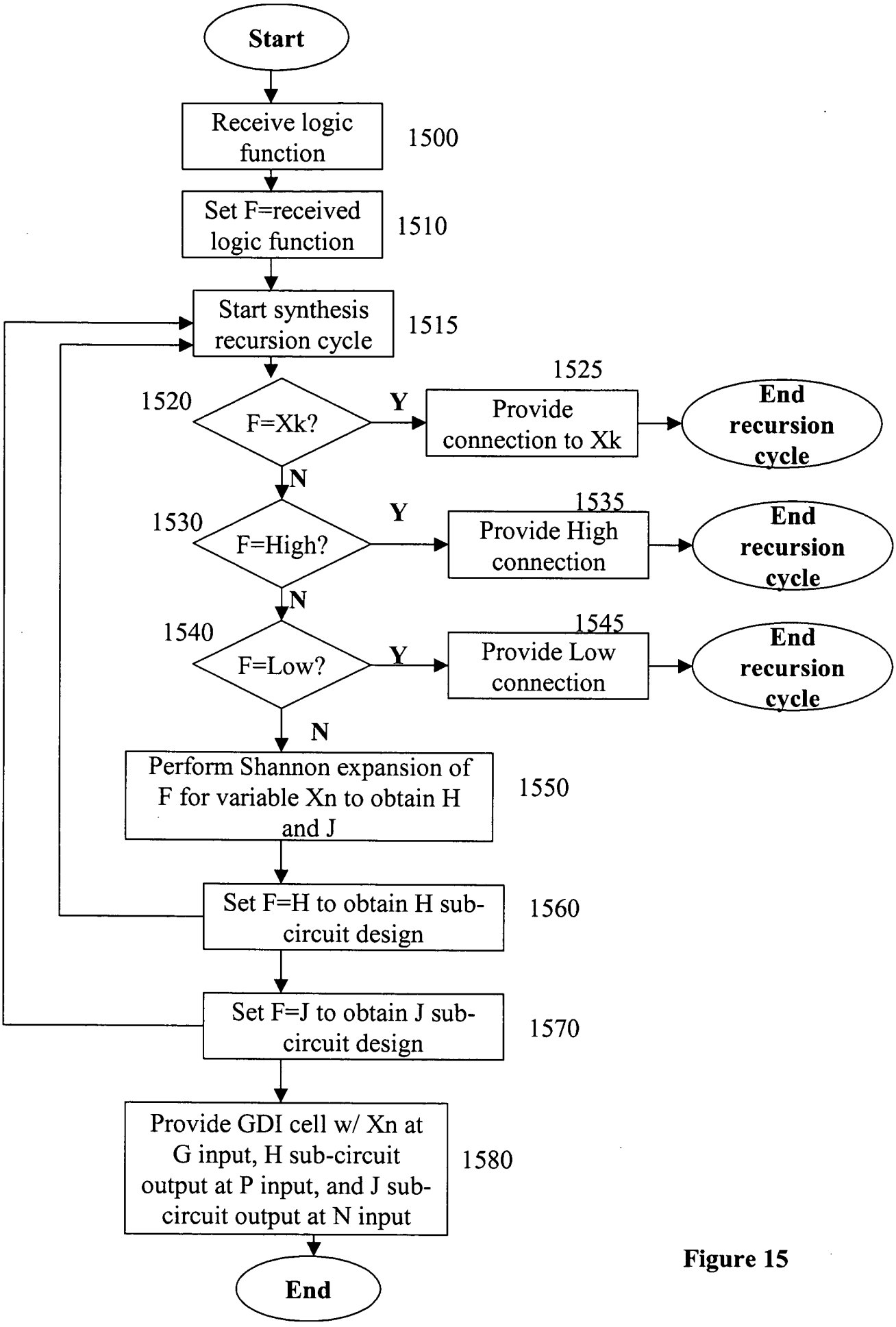

Start
Receive logic function
1500
Set F=received logic function
1510
Start synthesis recursion cycle
1515
1520
F=Xk?
Y
1525
Provide connection to Xk
End recursion cycle
N
1530
F=High?
Y
1535
Provide High connection
End recursion cycle
N
1540
F=Low?
Y
1545
Provide Low connection
End recursion cycle
N
Perform Shannon expansion of F for variable Xn to obtain H and J
1550
Set F=H to obtain H sub-circuit design
1560
Set F=J to obtain J sub-circuit design
1570
Provide GDI cell w/ Xn at G input, H sub-circuit output at P input, and J sub-circuit output at N input
1580
End

Figure 15

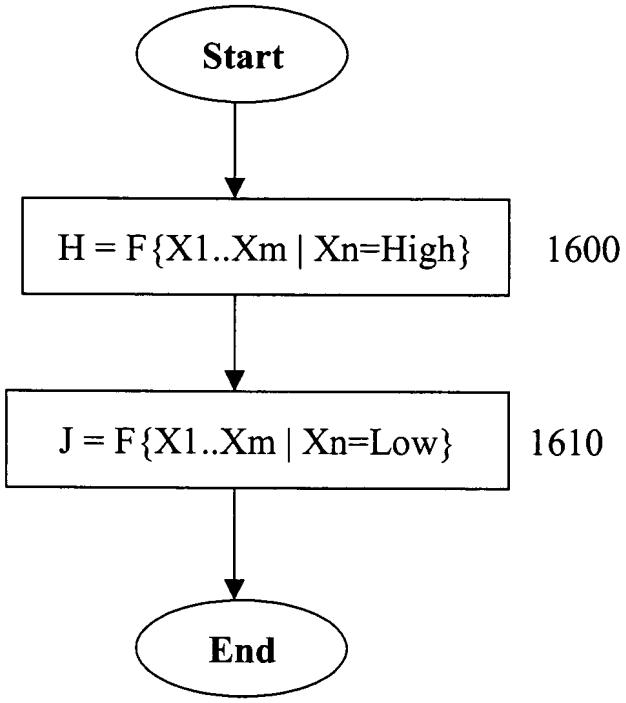


Figure 16

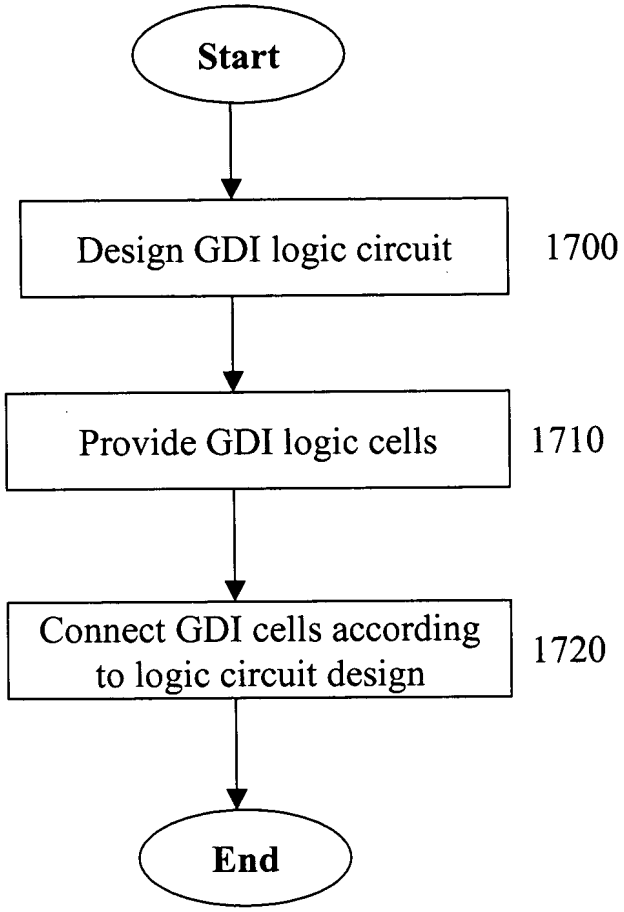
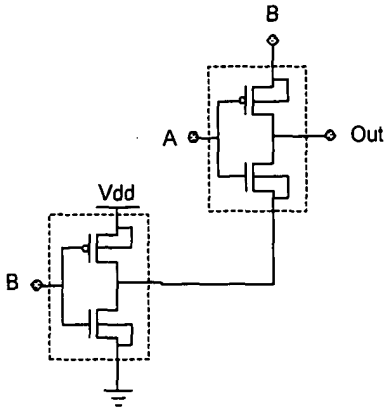
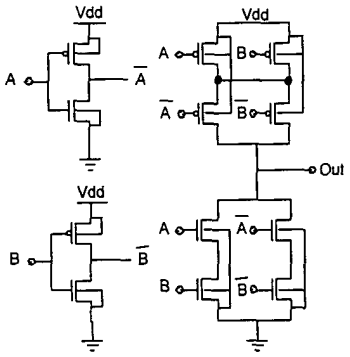

Start
Design GDI logic circuit
1700
Provide GDI logic cells
1710
Connect GDI cells according to logic circuit design
1720
End

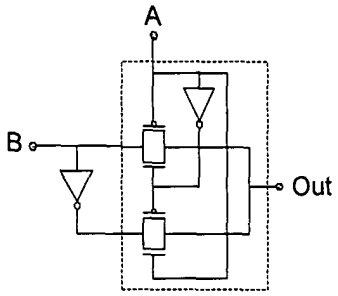
Figure 17



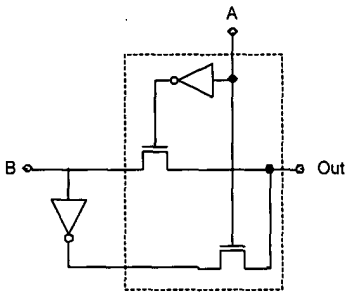
GDI
4 transistors



CMOS – Prior art
12 transistors



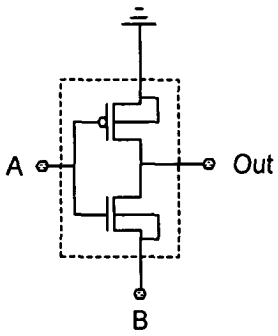
TG – Prior art
8 transistors



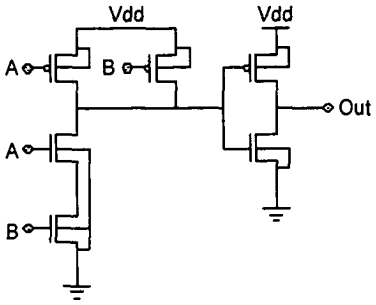
N-PG – Prior art
6 transistors

XOR gate

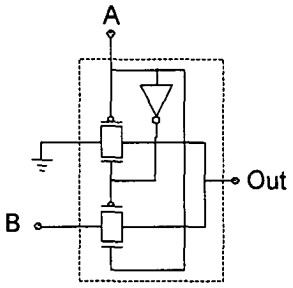
Figure 18a



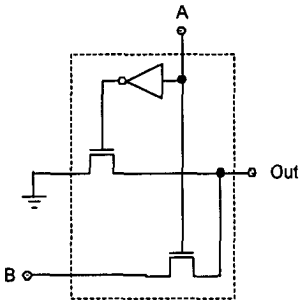
GDI
2 transistors



CMOS - Prior art
6 transistors



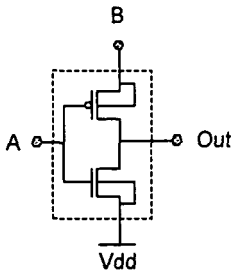
TG - Prior art
6 transistors



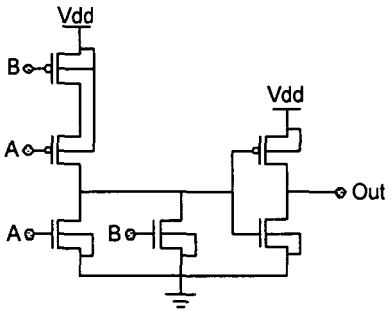
N-PG - Prior art
4 transistors

AND gate

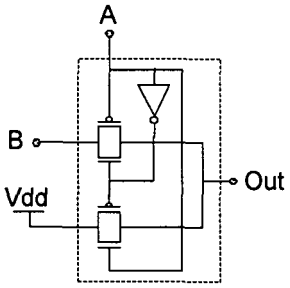
Figure 18b



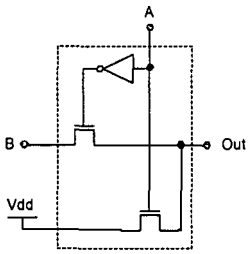
GDI
2 transistors



CMOS - Prior art
6 transistors



TG - Prior art
6 transistors



N-PG - Prior art
4 transistors

OR gate

Figure 18c

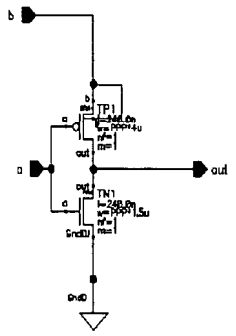
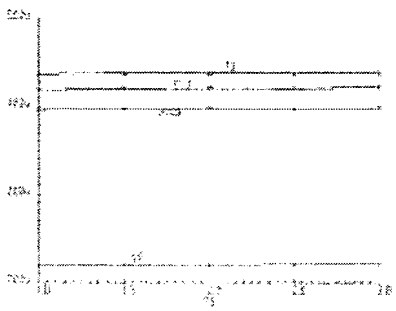
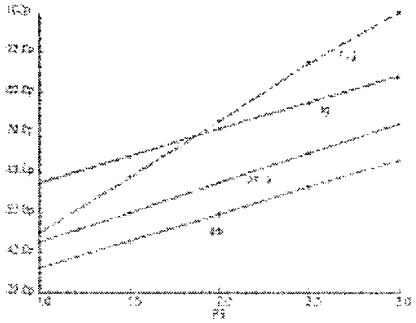
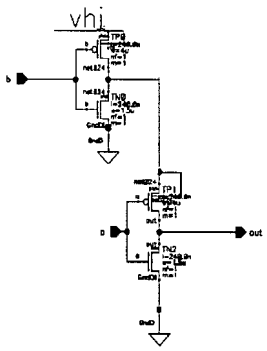
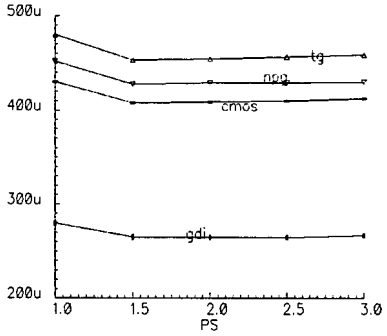
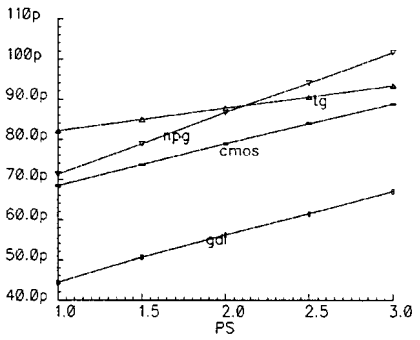
	GDI	Power (DUT and driver) vs. load size	Delay vs. load size
NOR			
AND			

Figure 19

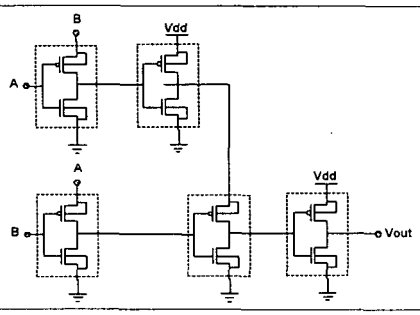
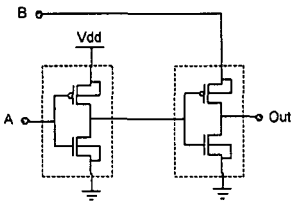
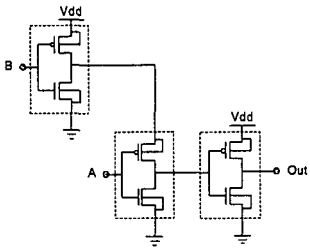
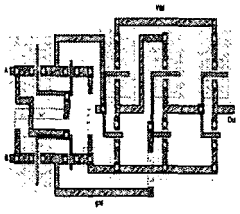
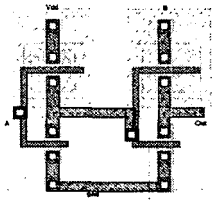
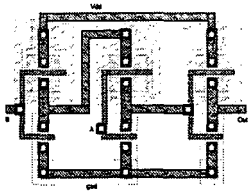
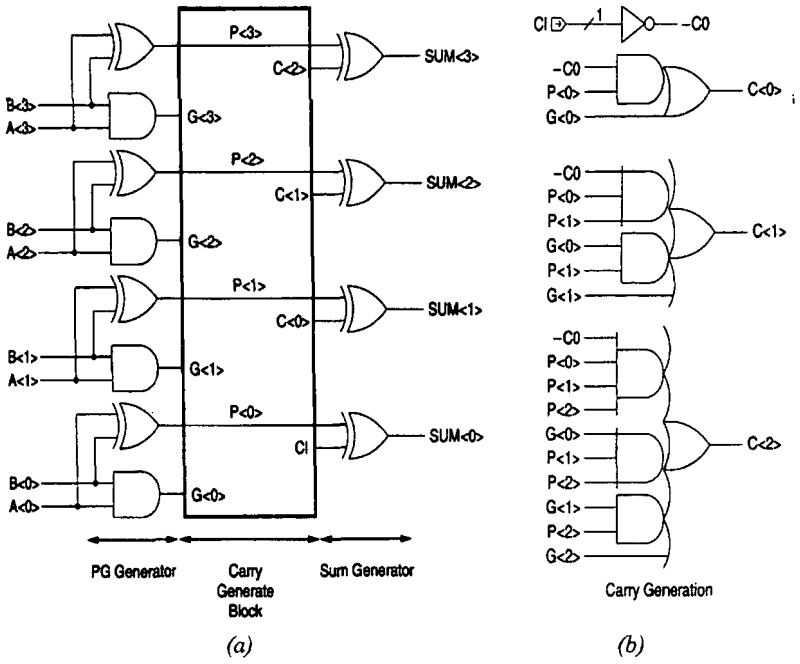
XOR	*AND*	*OR*
		
		

Figure 20



a) Basic scheme

b) Carry Generator (3-bit only)

Figure 21 – Prior art

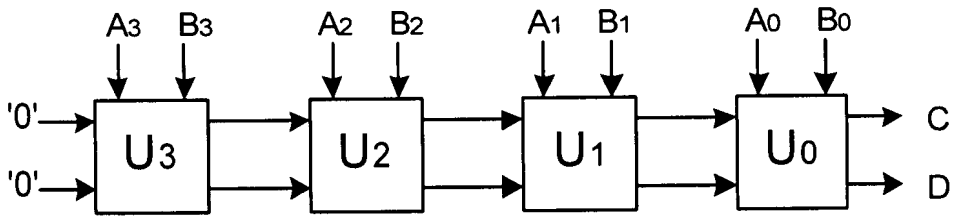


Figure 22 – Prior art

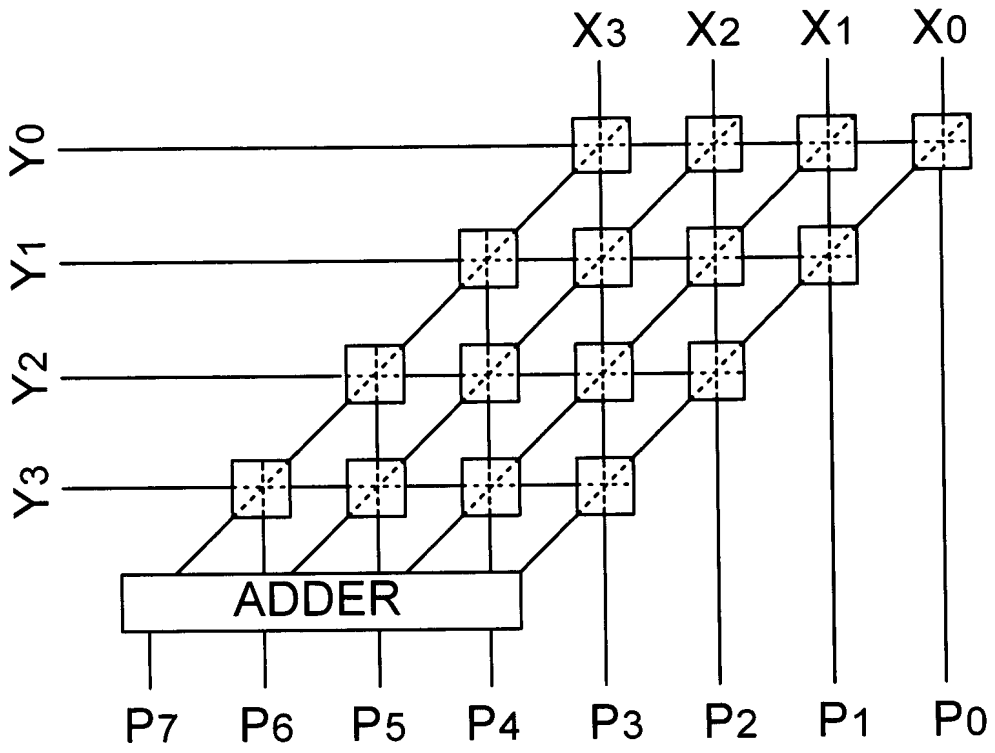


Figure 23 – Prior art

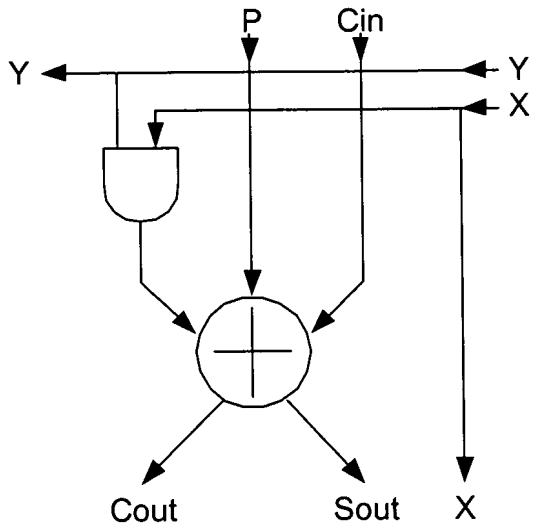
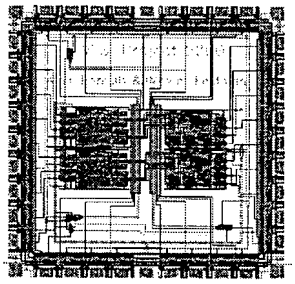
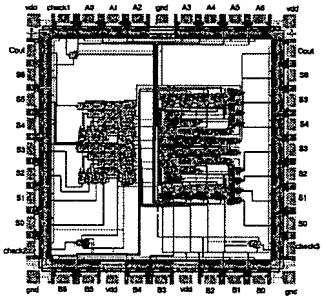


Figure 24 – Prior art



a) GDI and prior art CMOS



b) GDI and prior art TG

Figure 25

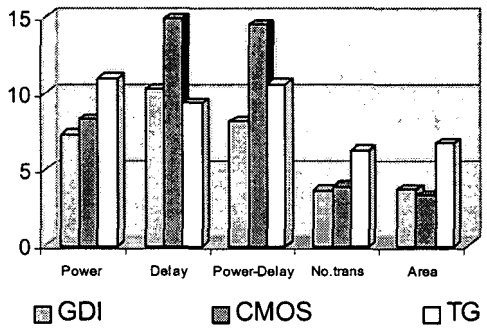


Figure 26

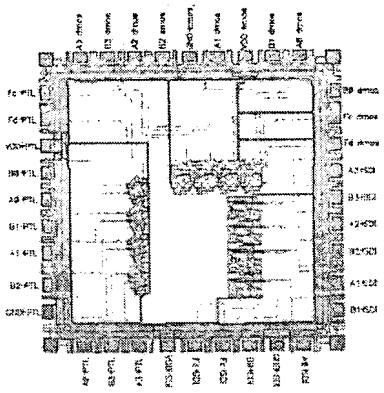


Figure 27

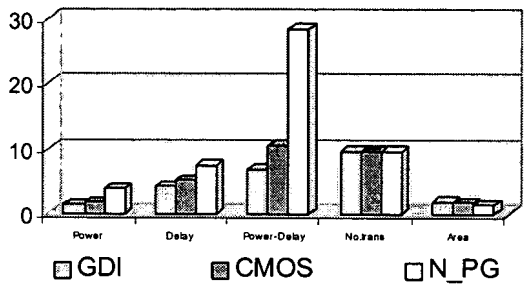


Figure 28

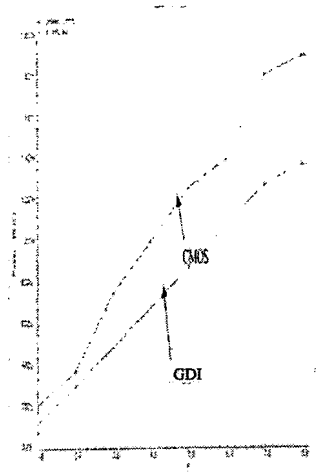


Figure 29

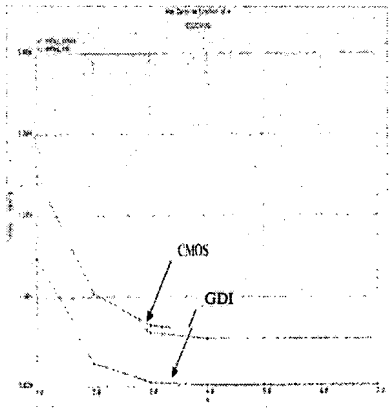


Figure 30

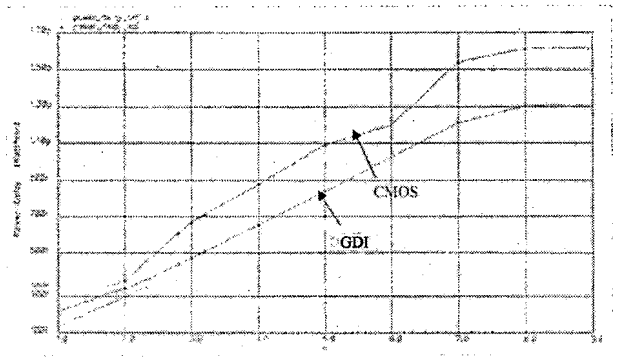


Figure 31

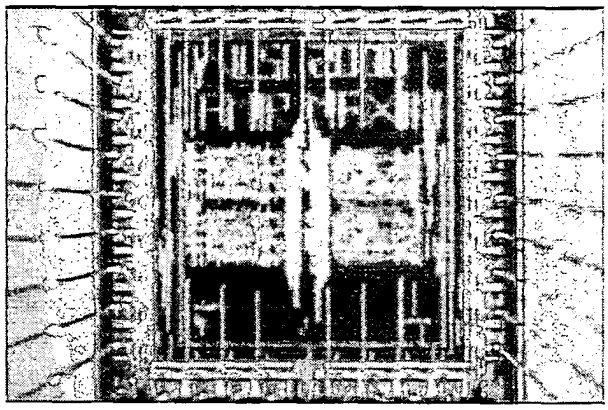


Figure 32

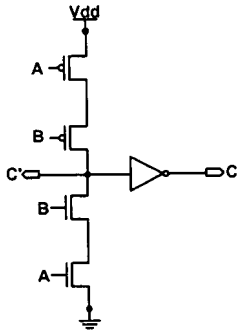


Figure 33a - Prior art

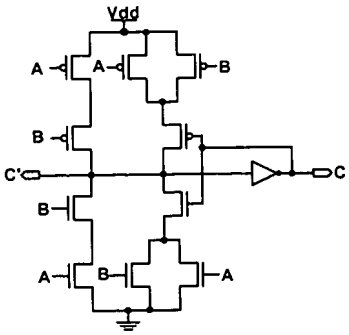


Figure 33b - Prior art

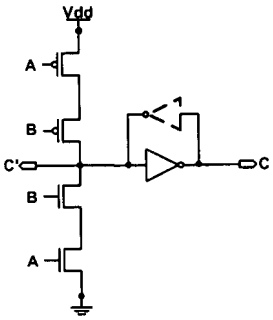


Figure 33c - Prior art

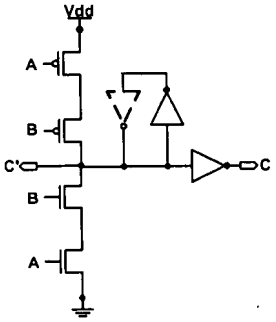


Figure 33d - Prior art

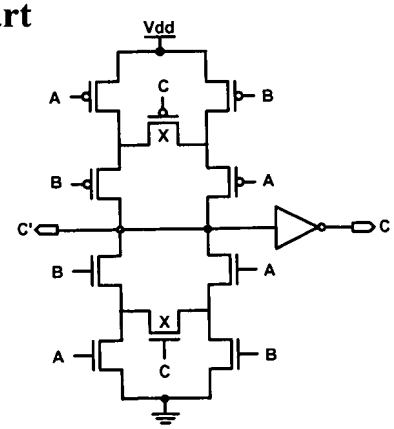


Figure 33e - Prior art

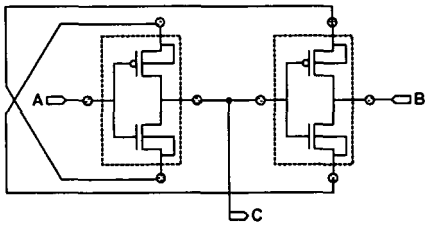


Figure 34a

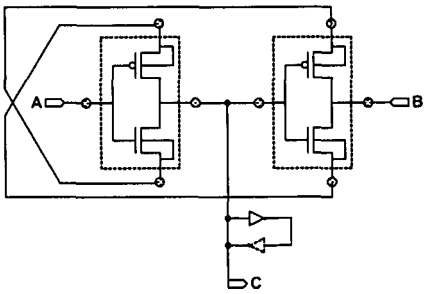


Figure 34b

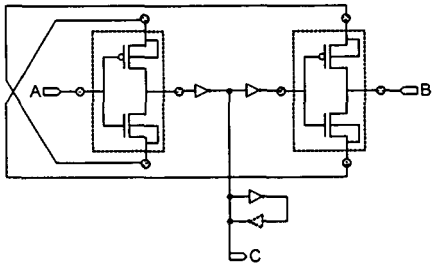


Figure 34c

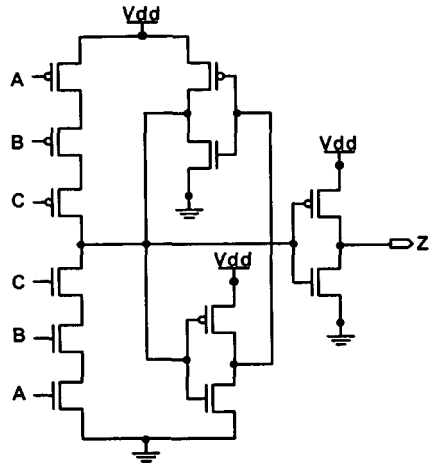


Figure 35a CMOS – Prior art

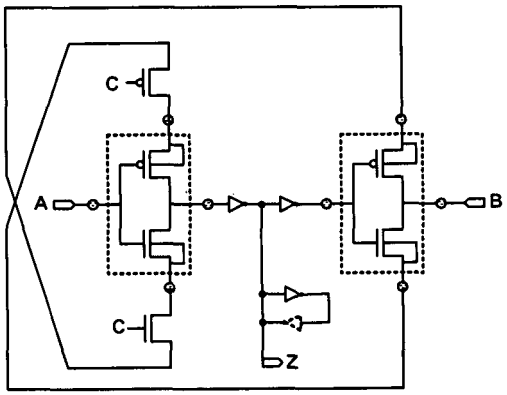


Figure 35b GDI

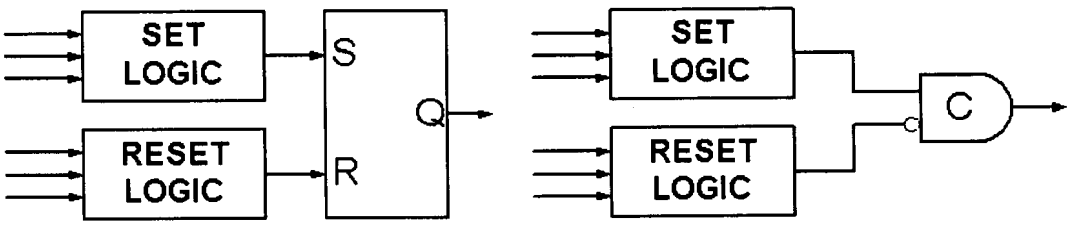


Figure 36 – Prior art

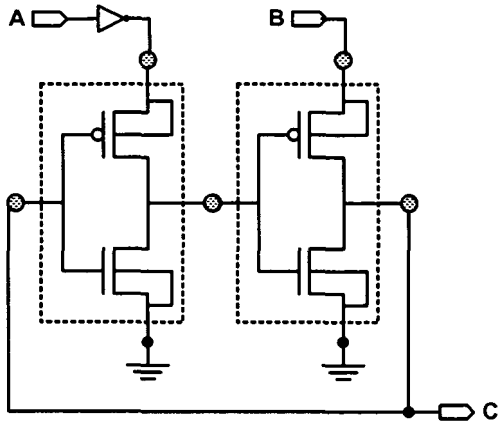


Figure 37a

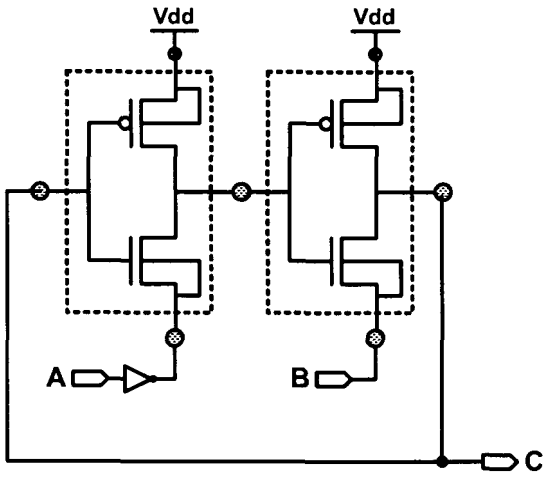


Figure 37b

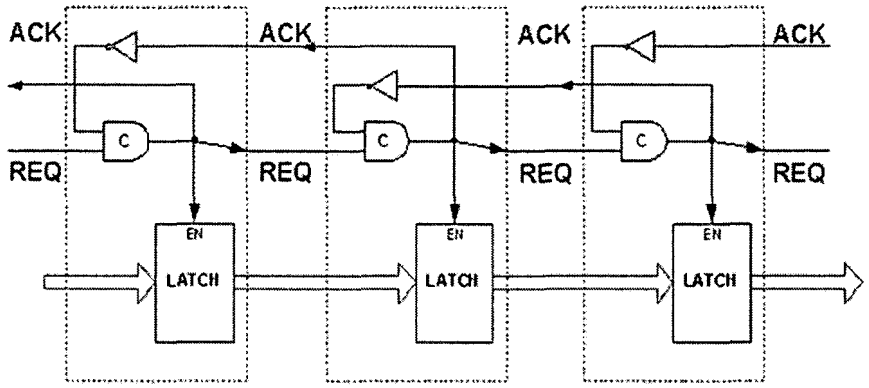


Figure 38 – Prior art

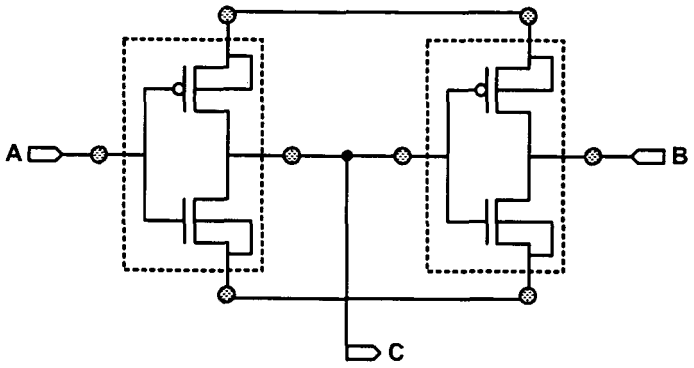


Figure 39

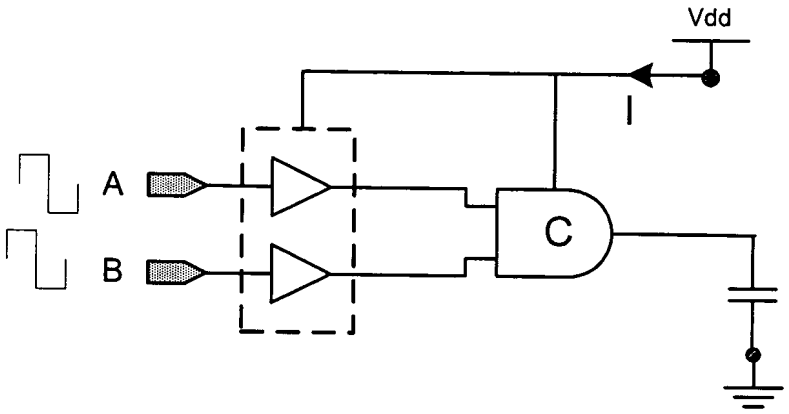


Figure 40

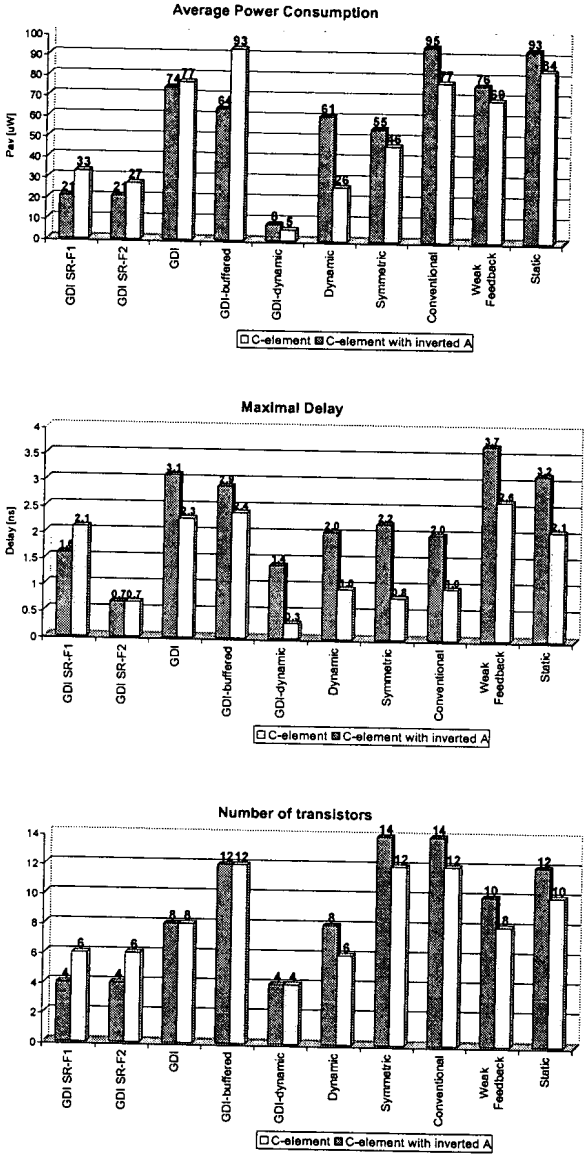

Average Power Consumption
Pav [uW]
100
90
80
70
60
50
40
30
20
10
0
24 33
24 27
74 77
64 93
6 5
61 25
55 45
95 77
76 69
93 84
GDI SR-F1
GDI SR-F2
GDI
GDI-buffered
GDI-dynamic
Dynamic
Symmetric
Conventional
Weak Feedback
Static
C-element
C-element with inverted A
Maximal Delay
Delay [ns]
4
3.5
3
2.5
2
1.5
1
0.5
0
1.6 2.1
0.7 0.7
3.1 2.3
2.9 2.4
1.3 0.3
2.0 0.9
2.2 0.8
2.0 0.9
3.7 2.5
3.2 2.1
GDI SR-F1
GDI SR-F2
GDI
GDI-buffered
GDI-dynamic
Dynamic
Symmetric
Conventional
Weak Feedback
Static
C-element
C-element with inverted A
Number of transistors
14
12
10
8
6
4
2
0
4 6
4 6
8 8
12 12
4 4
8 6
14 12
14 12
10 8
12 10
GDI SR-F1
GDI SR-F2
GDI
GDI-buffered
GDI-dynamic
Dynamic
Symmetric
Conventional
Weak Feedback
Static
C-element
C-element with inverted A

Figure 41

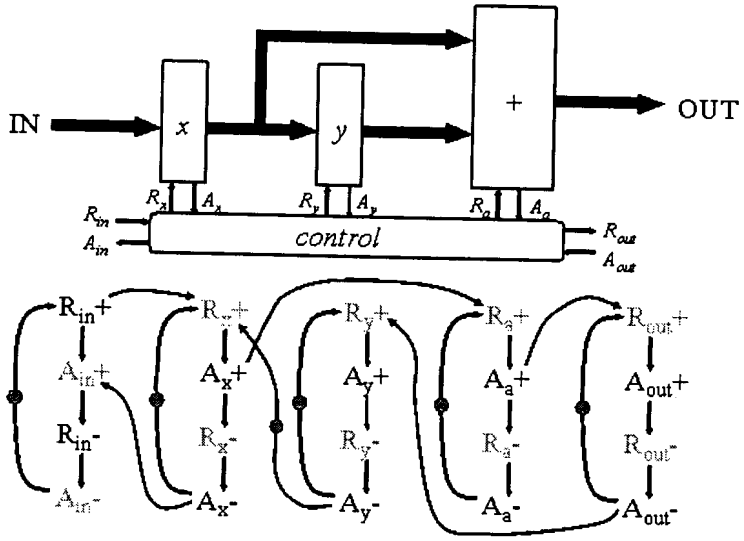


Figure 42 – Prior art

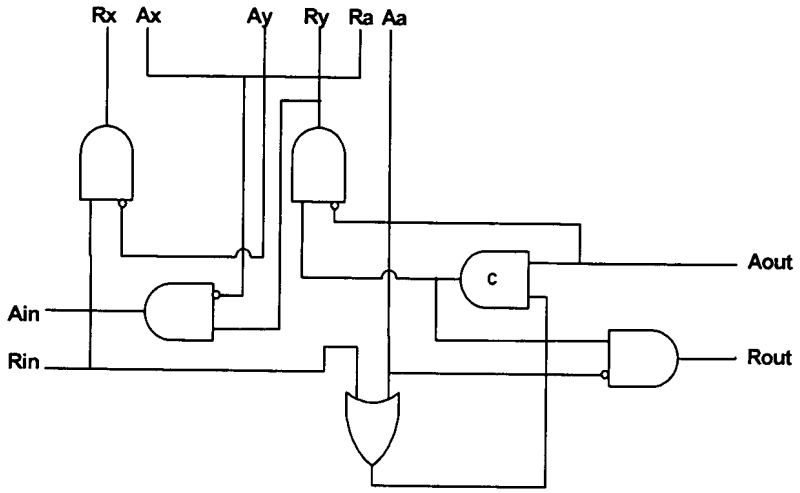


Figure 43a – Prior art

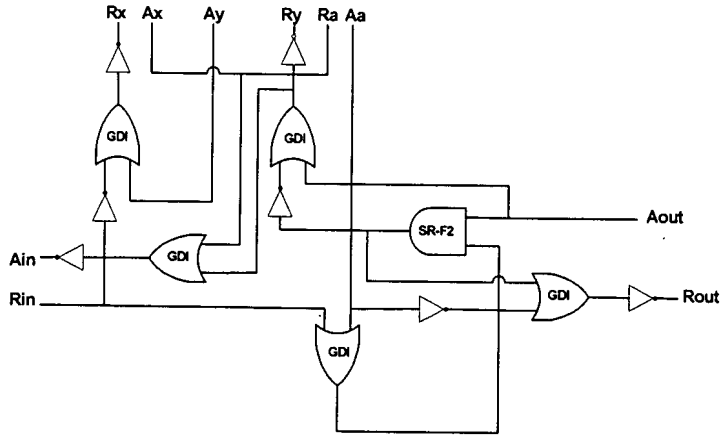


Figure 43b – Prior art

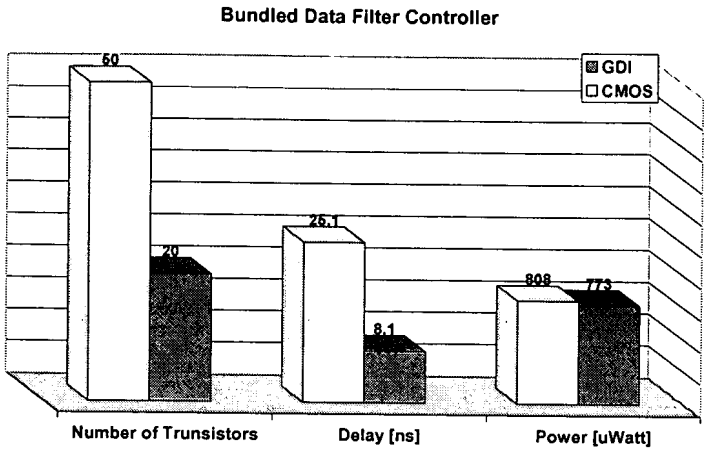

Bundled Data Filter Controller
GDI
CMOS
60
20
25.1
8.1
808
773
Number of Trunsistors
Delay [ns]
Power [uWatt]

Figure 44

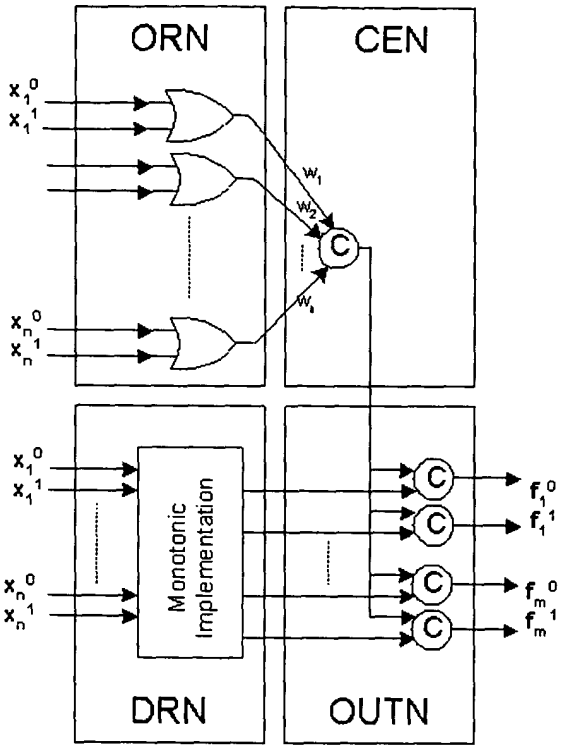
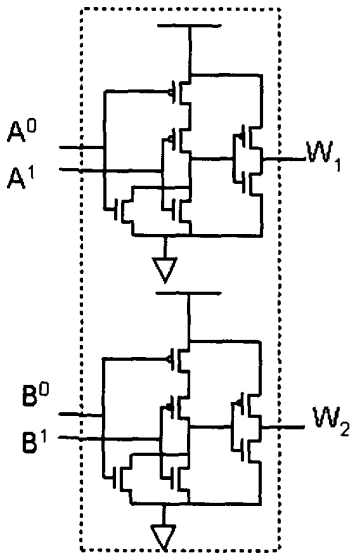
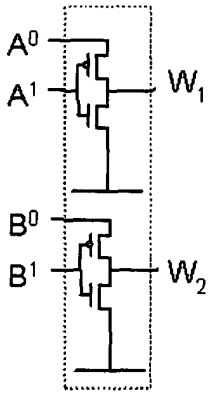


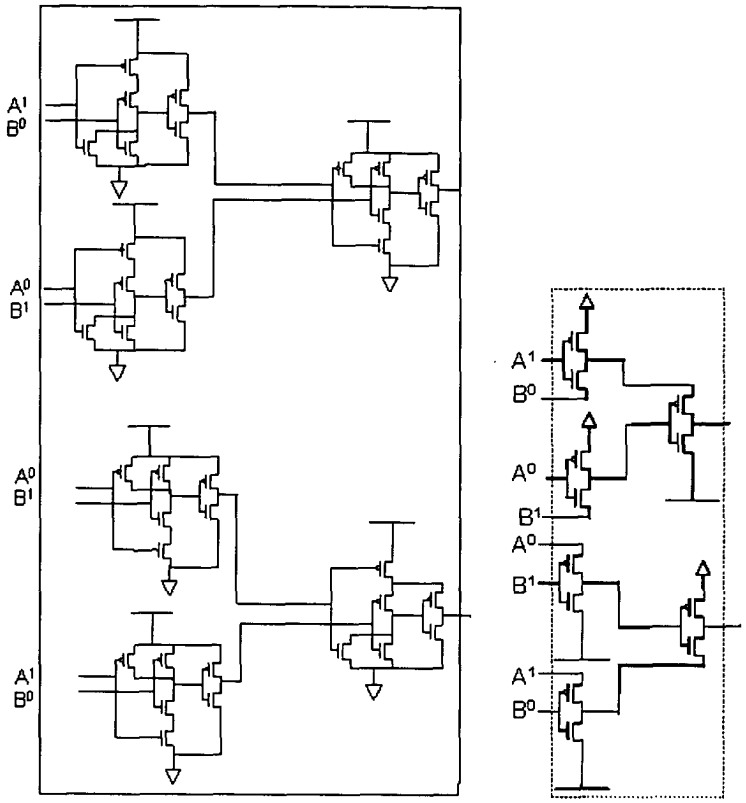
Figure 45 – Prior art





CMOS - Prior art **GDI**

Figure 46



CMOS - Prior art **GDI**

Figure 47

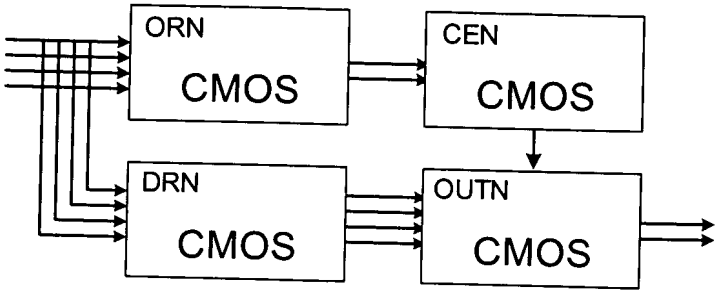


Figure 48a

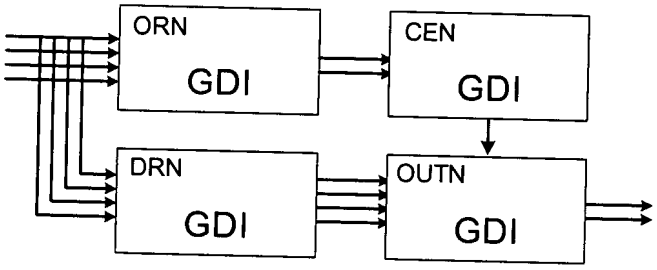


Figure 48b

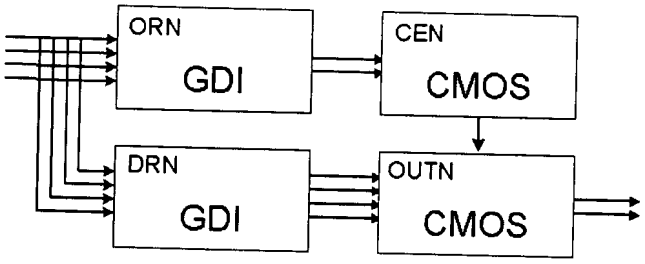


Figure 48c

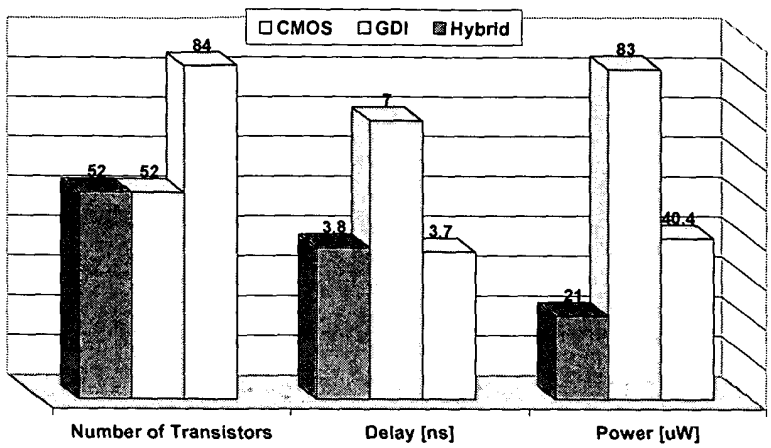
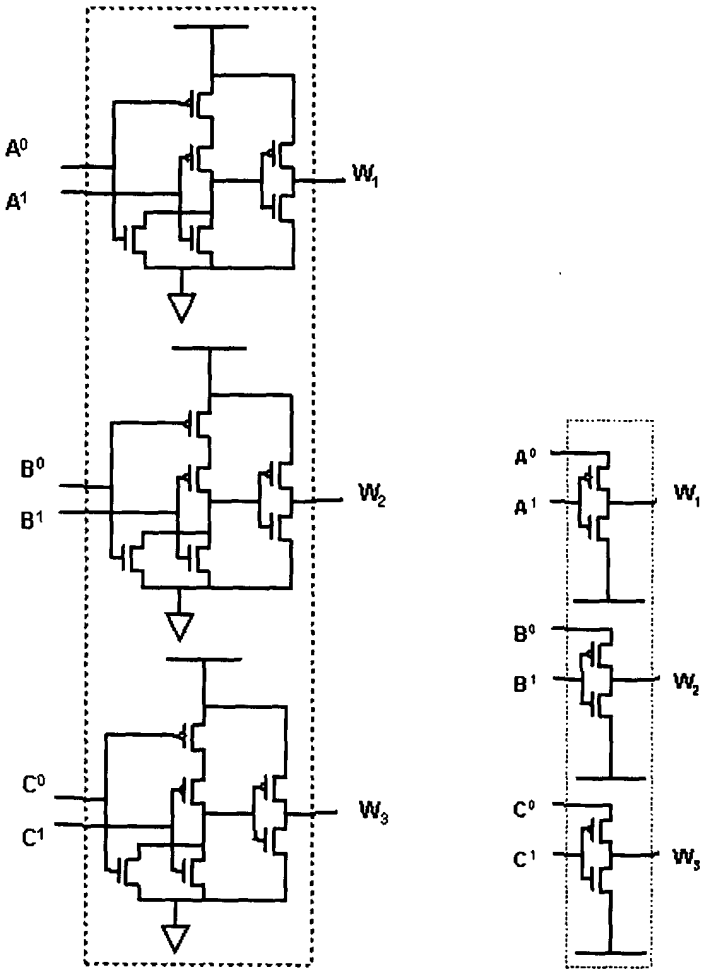

DR-ST XOR
CMOS
GDI
Hybrid
52
52
84
3.8
7
3.7
21
83
40.4
Number of Transistors
Delay [ns]
Power [uW]

Figure 49



CMOS - Prior art **GDI**

Figure 50

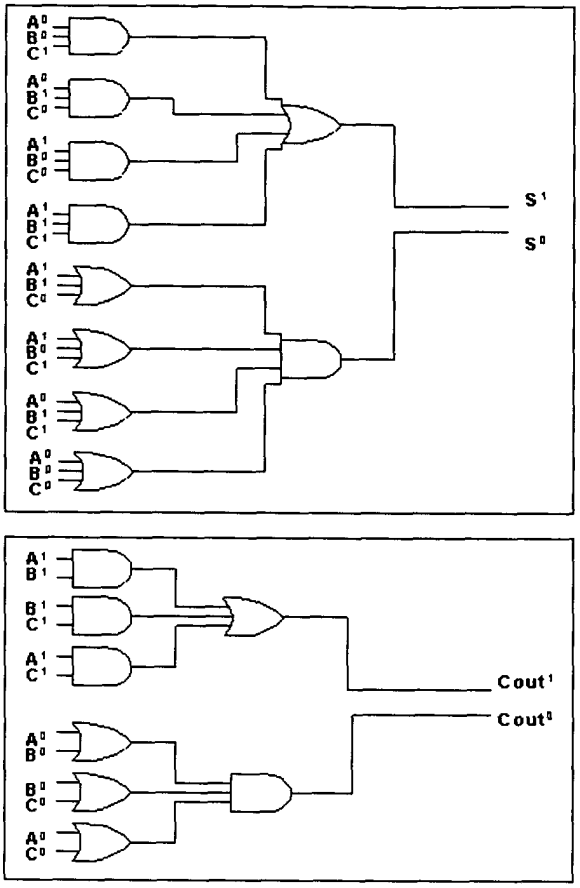


Figure 51 – Prior art

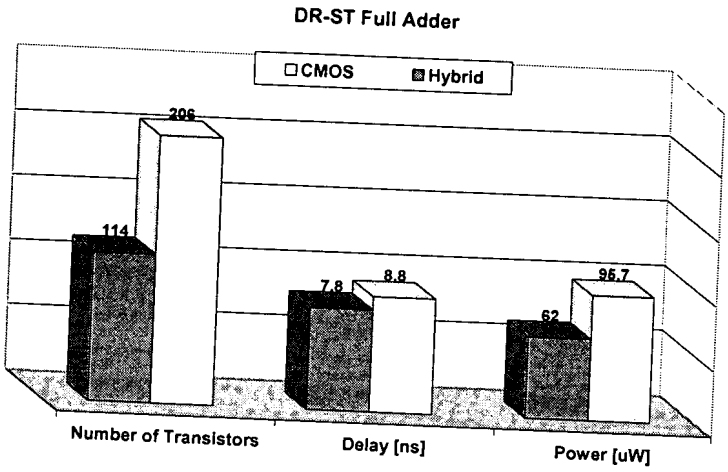

DR-ST Full Adder
CMOS
Hybrid
114
206
7.8
8.8
62
95.7
Number of Transistors
Delay [ns]
Power [uW]

Figure 52

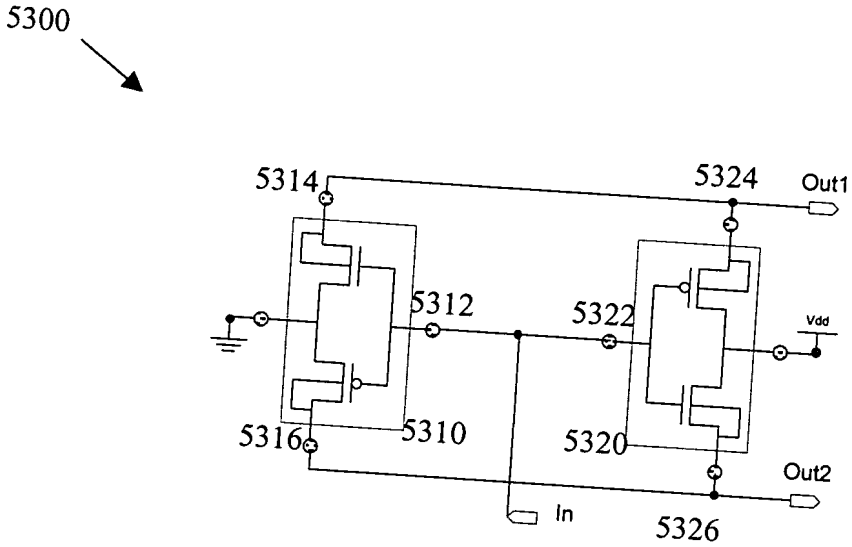


Figure 53